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Review

Silicon microtechnology and microstructures in separation science

Yolanda Fintschenko, Albert van den Berg*

MESA Research Institute, University of Twente, P.O. Box 217, 7500 AE Enschede, Netherlands

Abstract

The development of miniaturized total analysis systems, is driven by the desire to automate sample handling, separation or sensing, and detection of analytical instrumentation. Interest in planar structures for separation techniques, especially capillary zone electrophoresis (CZE), has grown rapidly. Initially most of those structures were realized in quartz, but recently polymers have been used to make planar microchannels. In spite of its attractiveness with respect to the potential integration of electronics and electrochemical and optical detectors, silicon has not been used very often, mainly because of its incompatibility with the high voltages used in CZE. In this contribution, an overview of the advantages and disadvantages of silicon for electroosmotically driven separation techniques is presented. Some silicon-derived insulating microstructures and their potential application in chemical analysis are also shown. The microtechnologies used comprise (deep) dry etching, thin-layer growth and anodic bonding. With this combination it is possible to create high resolution electrically isolating silicon dioxide structures with aspect ratios similar to those possible in silicon. Besides these channel structures, a capillary connector is presented with a very low dead and mixing volume for use in (correlation) electrophoresis, and tested by means of precision of consecutive single injections. Finally, the potential of integrated optical detectors in combination with micro-separation structures is presented.

Keywords: Reviews; Silicon microtechnology; Instrumentation; Detection; MicroTAS; Microchannels; Microfabrication; Silicon

Contents

*Corresponding author.

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1. Introduction

The advent of high-throughput screening for drug discovery and its potential in clinical analysis has increased interest in miniaturizing analytical techniques. Miniaturized total analysis systems (μTASs) are instruments where the sample handling, analysis and detection are integrated into a miniaturized system. The primary tool for the analytical chemist remains separation. Miniaturization decreases the analysis time while increasing the number of theoretical plates, decreasing band broadening, and decreasing sample consumption and waste production [1]. Microfabrication of these devices using microtechnologies such as photolithography, dry and wet etching offers the advantages of precision at the micron and sub-micron scale, the integration of detectors and other modules, and a vehicle for mass production.

High-performance liquid chromatography (HPLC) has been reported by MacNair et al. in 30 μm diameter capillaries [2]. Separation efficiencies of $2\cdot10^{-5}$–$3\cdot10^{-5}$ were achieved with total run times of 10–30 min [2]. Capillary electrochromatography (CEC), which uses an applied electric field to 'pump' solution by electroosmotic flow, has been shown to achieve the same results without the disadvantage of high pressures [3]. It requires high voltage power supplies, but no moving parts. Separation is affected in capillary zone electrophoresis (CZE) by differences in the mobilities of analytes in an applied electric field. By packing the capillary or modifying the walls and/or buffer, chromatographic interactions are introduced [4]. Electroosmotic pumping is therefore uniquely well-suited for the miniaturization of CZE and chromatography.

In 1992, Manz and co-workers reported the first demonstrations of capillary electrophoresis on a chip [5,6]. By etching small diameter channels in planar glass substrates (chips), Manz and co-workers integrated the injector with the separation channel on one structure [5,6]. Other structures described by Jacobson et al. were capable of making entire separations in a total of 150 ms [7]. CEC on a chip has also been demonstrated by Jacobson et al. using modified buffers or modifications to the channel wall itself [8]. The impact of CZE 'on a chip' is the elevation of separation techniques to quasi-continuous, generic chemical sensors.

2. Materials for planar capillary zone electrophoresis

Quartz glass has been the material of choice for planar CZE [6,9]. It is an insulator with a high breakdown voltage, and is optically transparent for UV light. Deviations from Ohm's law due to Joule heating occur at about 250 V/cm (1 mW dissipation maximum) for planar glass structures, the same values as observed with fused-silica capillaries [10]. Heating results in band broadening and limits the electric field strength that can be practically applied. The main practical disadvantage of glass as a substrate from a microfabrication standpoint is that can only be chemically etched isotropically. Therefore the options for the channel geometry are limited to elliptical channels. Additionally, the commercially available detectors typically used with CE, UV and fluorescence, have detection windows designed for a columnar rather than planar geometry. Laser-induced fluorescence (LIF) detectors have been the method of choice for detection in planar CZE, but these must be built. The ideal solution is to have an integrated detector, but this requires processing in silicon rather than glass.

Plastics have been also been used as substrates for planar CE. An anisotropically etched silicon mold was successfully replicated in poly(methyl methacrylate) (PMMA) and used for a CZE immunoassay [11]. Ohm's law plots for PMMA microchannel chip were similar to a fused-silica capillary of similar cross-sectional area [12]. The electric field strength maximum was 1100 V/cm with no breakdown observed. Other researchers have obtained narrow channels from poly(dimethylsiloxane) (PDMS) molded against a microfabricated silicon master for the analysis of DNA restriction fragments and single DNA molecule detection [13]. The advantages of working in polymers include low cost, high E-field strengths, and improved heat dissipation. However, the structures reported in the literature rely on an anisotropically etched silicon template [11–13]. An alternative to this is to use a dry etched silicon microstructure, electroplate an intermediate nickel mold, and use this structure to make plastic microstructures using hot embossing [14]. With this technique, a larger freedom is the microchannel cross-section is obtained.

Webster and Mastrangelo reported using a silicon

platform for CE on a plastic chip in 1997 [15]. By using a silicon platform, a diode detector was integrated into a channel made by depositing *p*-xylylene and polyimide on the silicon platform. This configuration was evaluated using fluorescently labeled DNA. The limits of detection and separation efficiencies were not evaluated, rather the performance of the detector was reported for a 0.5 μg/μl sample of DNA. The channel dimensions were larger than those typically reported, with widths at 200 μm. The novelty of this system lies in its total integration of electrodes for high voltage application, a channel for separation, and diode detector. The channel itself was filled with gel.

The large variety of micromachining techniques available for silicon [16] makes it a very attractive material for CZE applications. Unfortunately, silicon is a semiconductor, and the thin films usually used for its electrical insulation do not withstand the high voltages needed for an efficient and fast separation [17]. The so-called ground plate supported insulating channel (GPSIC) method was developed to overcome this drawback [18]. Channels are etched in silicon using wet or dry chemical etch methods, then passivated. The channels are sealed by anodically bonding to a glass substrate. The remaining silicon is removed from the back of the channels by wet chemical etching. The surface area of channels etched in silicon can be increased by making porous silicon or silicon black [19,20]. The end result is a channel of high surface area suitable for chromatography. A combination of porous silicon with the GPSIC methodology is a promising substrate for CEC.

3. Microfabrication technologies

The etch methods for silicon are classified under four categories: wet anisotropic, wet isotropic, dry anisotropic and dry isotropic [16,21]. For wet anisotropic etching, basic solutions of KOH in water are mostly used. The anisotropic etch rate is higher in the (100) crystal plane than the (111), the relationship being determined by the etch solution (e.g. potassium hydroxide, cesium hydroxide). The shape of the anisotropically etched structures is determined by the slow-etching (111) crystal planes of the silicon. For wet isotropic etching aqueous acidic solutions containing HF and HNO_3 are necessary. The composition of the solution determines the final shape of the channel. Isotropic etching occurs at the same rate in all directions. Loading effects resulting from the diffusion limited etching process apparently form a major drawback of this technique, since they reduce the homogeneity of etched channels over the wafer. However, these effects can be overcome by the addition of compensation structures to the microstructure design [22]. First results with these compensation structures resulted in a lowering of the channel diameter variation over one wafer by a factor of 2.

For dry etching, a plasma etching machine is used. By varying the etching conditions, the shape of the channels can be varied from perfectly isotropic to directional. Also positive or negative tapering is possible [23]. The basic approach for constructing channels in silicon is as follows: the silicon ({100} oriented) is covered with a mask material, the mask material is patterned, and the silicon is etched using one of the methods described above. Fig. 1 schematically shows the geometries of three etch procedures. The channel on the right of the picture is etched isotropically, the middle anisotropically using reactive ion etching (RIE), and the channel on the left is etched anisotropically in a KOH solution. After etching there are a number of ways to proceed, depending on the desired channel configuration. The simplest way to close the channel is by anodically bonding it to Pyrex glass.

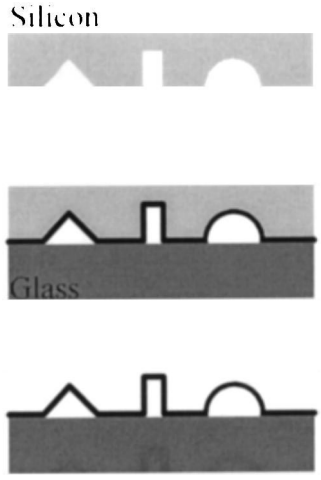

Fig. 1. Process for ground plate supported insulating channels.

4. Microstructures for separation fabricated using silicon-based technologies

4.1. Ground plate supported insulating channels

The GPSIC fabrication sequence is shown in Fig. 1. First the channel is etched in silicon. The etching process can be isotropic or anisotropic. The mask material is removed and the channel is covered with two thin layers of low pressure chemical vapor deposition (LPCVD) silicon nitride (50 nm) and silicon oxide (tetraethyl orthosilicate, TEOS, max. 600 nm) respectively. The silicon oxide is needed to be able to bond the wafer anodically to a glass wafer (a wafer covered with silicon nitride can not be bonded anodically). After bonding, the silicon wafer containing the channels is etched away using an isotropically etching solution, leaving the free standing silicon nitride. The etch-back can also be done using an anisotropic etching solution. In this case an extra layer of polysilicon has to be applied before applying the silicon-nitride and -oxide layer, to prevent the appearance of 'left-over' silicon in corners due to the anisotropic etching.

To avoid bonding as well as the fragile covering of the channels described above, a method to etch channels beneath the surface of the wafer ('buried channels') was developed. The procedure is related to the method used by French et al. [24] to make isolated resistor islands for use in a single crystal silicon piezoresistor. They etched narrow trenches (2 mm wide, 10 mm deep) crossing each other perpendicularly in the plane of a silicon wafer, using a RIE process. After that they immersed the wafer in a KOH solution to yield channels that were partly buried beneath the surface. To insulate the islands that appeared, they oxidized the silicon until a thick layer of oxide was formed.

The method employed here is as follows [22] (Fig. 2 right): First, a deep, very narrow trench (typically 100 μm deep, 4 μm wide) is etched using RIE etching. After that, the surface of the wafer is covered with a layer of silicon nitride. This nitride also covers the walls and the bottom of the trench. Then the silicon nitride in the bottom of the trench is etched away using RIE etching, leaving the bare silicon. Next, the wafer is etched using one of the methods described in the beginning of this chapter.

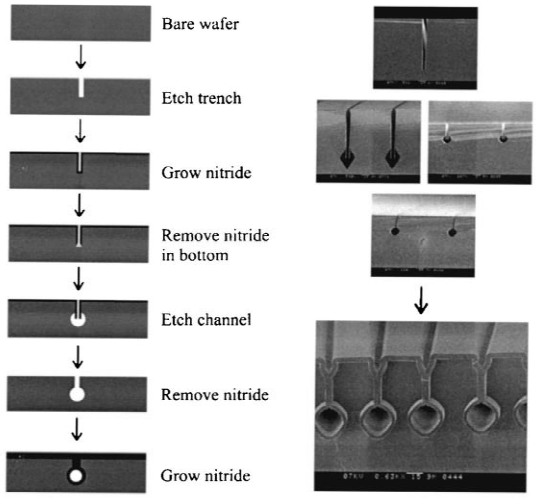

Fig. 2. Process sequence (left) and SEM micrographs (right) of buried channels (from [22]).

The nitride is removed by etching in 50% HF. The last step consists of the deposition of a thick layer on the wafer, that covers the walls of the channel, and also of the trench. The deposited layer is thick enough to close the trench. The materials that can be used for the layer are silicon oxide, silicon nitride, and polysilicon. In the examples presented here LPCVD silicon nitride was used. In Fig. 2 (left) some examples of realized buried channels are shown.

Examples of GPSICs are shown in Figs. 3 and 4. The GPSIC process leaves channels with a user-determinable shape (they can be etched isotropically or anisotropically, using an isotropic etching solution or RIE etching), which are transparent, so they can be used in an optical detection system. The wall thickness (<1 μm) facilitates rapid cooling, which would enable working at higher electric field strengths without seeing deviations from Ohm's law. The addition of the protection/planarization layer over the channels improves their practical usefulness. Several layers/materials such as thin films, polymers, and glue can be applied for this purpose. If a transparent material is used, the whole structure remains transparent from the top and the bottom side, which allows for optical detection methods.

GPSICs can also be constructed using the buried channel etching method. For this, after closing the

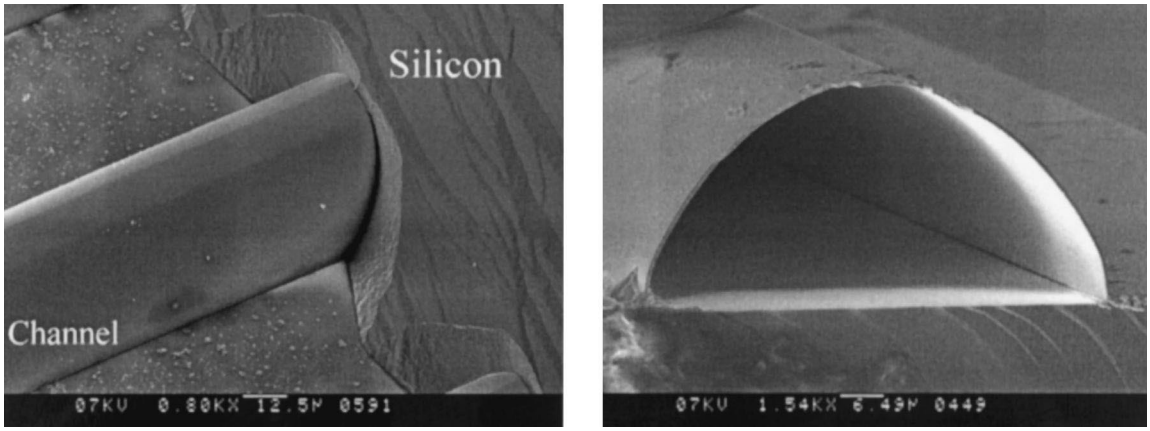

Fig. 3. SEM micrographs of isotropically etched microchannels fabricated with the GPSIC.

trench with silicon nitride, a layer of silicon oxide was deposited to facilitate bonding to a glass wafer. After bonding, the silicon wafer was etched away, leaving the free- standing channels. Disadvantages of the buried channel etching method are its complexity and the fact that special equipment is necessary, e.g. an RIE with high density source and cryogenic cooling.

4.2. Silicon black

As stated earlier, CEC currently receives a lot of attention, as it promises to combine the advantages of capillary electrophoresis and liquid chromatography [25]. In CEC, separation takes place in a packed column using electroosmotic flow (EOF) instead of pressure as the driving force. When miniaturizing CEC structures, one of the difficulties is to pack the microcolumn [26]. For this reason there is an interest in preparing high surface area structures that do not need to be packed. One possibility is to use the so-called silicon black technique, that enables the fabrication of (sub)micron size columnar structures with a very high surface area (see Fig. 5) [23]. Since the surface of these structures consists of SiO_2, commonly known chemistries can be use for derivatization of the

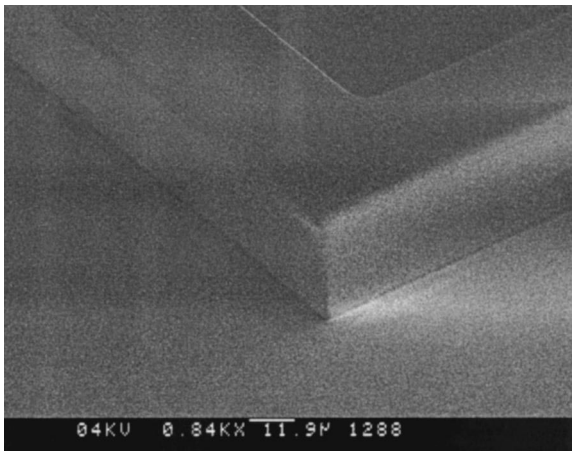

Fig. 4. SEM micrograph of a DRIE-based GPSIC.

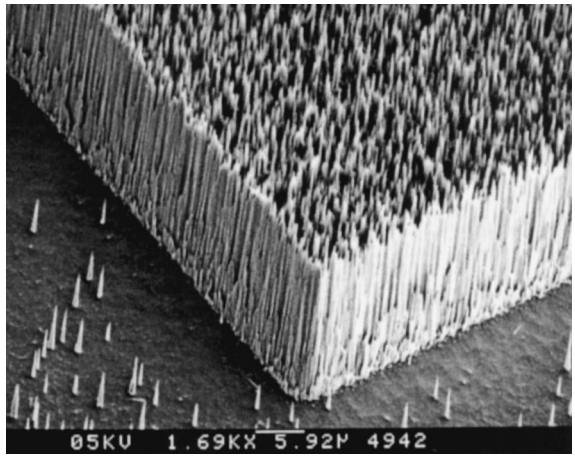

Fig. 5. ‘Micrograss’ formed by the silicon black method (from [23]).

structures. The main problem using these structures in practice is the reproducibility of the surface area, and the ruggedness of the microstructures.

4.3. Porous silicon

An alternative method to produce a high surface area packing in silicon is to use electrochemical etching for the fabrication of porous silicon. The pore size of the porous silicon can be controlled by the experimental conditions of the anodization. Porous silicon has been widely investigated for a variety of applications, such as use as sacrificial layer [27,28], silicon-integrated light source [29], material for moisture sensing [30], high surface area matrix for biosensing [31], and diffusion barrier in a micro reference electrode [32]. A particularly interesting property of porous silicon is its large internal surface area of up to 600 m^2/cm^3 [33], which, in combination with its straightforward chemical functionalization, makes it an attractive candidate for CEC application. Although porous silicon films can be easily spatially defined on a silicon wafer, the great challenge is to develop a technology which enables the integration with already formed microseparation channels. The main difficulty here is the problematical application of photolithography after formation of the porous silicon.

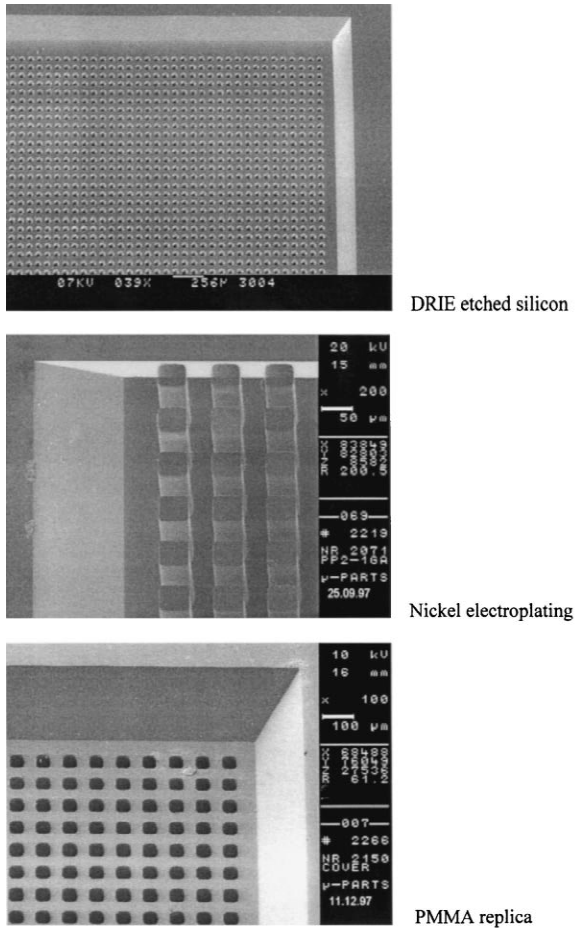

Fig. 6. Examples of three subsequent structures made in the DEEMO process.

4.4. Dry etching, electroplating, molding

DEEMO (dry etching, electroplating, molding) is a silicon derived technique for the fabrication of polymer microstructures [14]. It involves the microstructuring of silicon using deep reactive ion etching (DRIE), (nickel) electroplating, and plastic molding. Contrary to the well known LIGA technique that uses expensive synchroton radiation to create high aspect ratio, three-dimensional structures, in DEEMO deep dry etching is used to create three-dimensional structures. Dry etching has considerable advantages over alternative high aspect ratio processes such as deep UV-lithography, laser ablation, ion milling, spark erosion, and is much cheaper than the Lithografie Galvanoforming Abformung (LIGA) process. DEEMO features low initial cost and a fast prototyping cycle, whereas the structural definition of the silicon mold (μm range) is less than using synchroton radiation (nm range). However, in most practical cases the precision obtained with DEEMO is largely sufficient. Fig. 6 shows mold inserts fabricated by means of dry etching, subsequently electroplated nickel structure and embossed PMMA structures (produced in cooperation with Micro*Parts, Dortmund, Germany). Compared to earlier published embossed structures made using anisotropically etched silicon molds, DEEMO offers a much greater flexibility in three-dimensional structures.

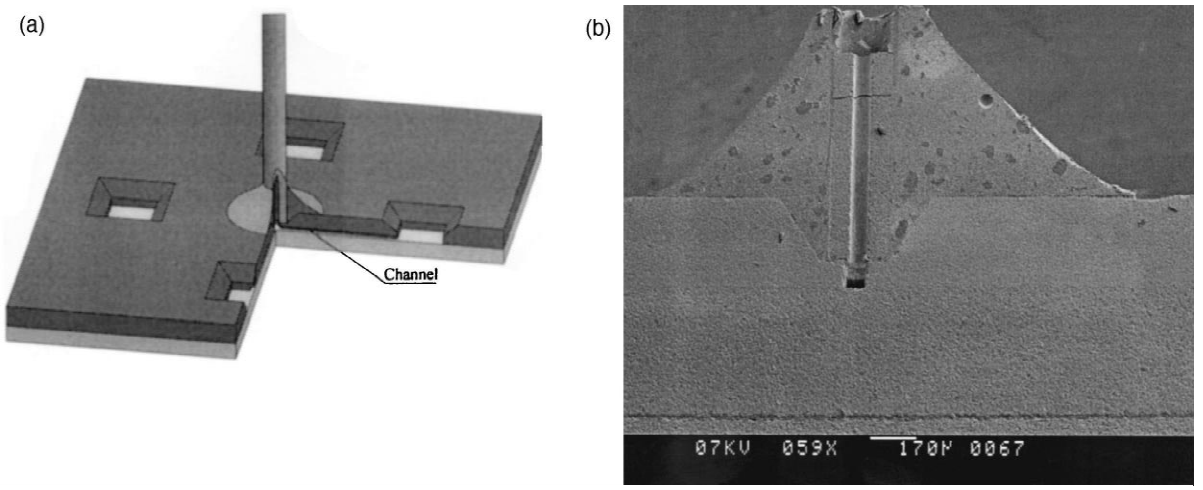

Fig. 7. (a) Capillary connector combined on-chip with sample injector holes (from [35]). (b) Cross-section of glued 280/75 μm (O.D./I.D.) capillary (from [35]).

5. Other silicon-based components

5.1. Capillary connector

Connections between a capillary and the sample injector or between several capillaries are realized via micro channels in silicon. The capillary connection chips were designed and fabricated by Twente MicroProducts (Enschede, Netherlands). The sample injection holes, channels, and wafer-through holes are realized by both dry and wet etch methods. The channel dimensions are matched to the inner diameter of the capillary, thus minimizing the dead and mixing volume of the connection. The channels are electrically isolated with a thin layer of silicon oxide and they are covered by a glass plate. The electrically isolated connectors are fabricated in a very reproducible way. Essential for a suitable connection are the application of high-performance dry etch techniques, the design of a prealigned connection, and the gluing technique.

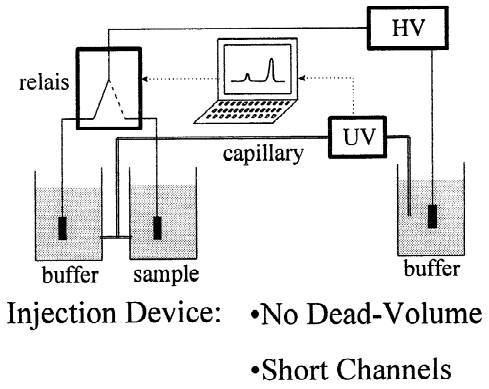

Fig. 8. Correlation CZE system (from [35]).

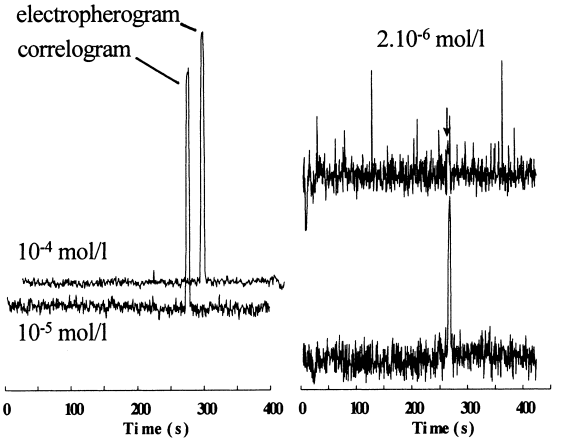

Fig. 9. Electropherogram vs. correlogram (from [35]).

Fig. 7 shows a diagram and a scanning electron microscopy (SEM) of a cross-section of a glued capillary connection with a microchannel. Fig. 8 shows a photograph of the microconnector incorporated into the correlation CZE apparatus. The dead volume was less than 0.5 nl, and the alignment was within 5 μm. The structure was able to sustain voltages up to 250 V/cm across the channel, and pressures up to 120 bar.

The connector has been tested by using a set-up for correlation electrophoresis as described in [34]. After proven precision of eight consecutive injections the so-called correlation capillary zone electrophoresis (CCZE) technique was applied [35]. The capillary connector showed reproducible behavior (R.S.D. values<1%). The results in Fig. 9 show the improvement of the limit of detection as a result of the CCZE technique. A comparison of the typical electropherogram to the correlogram shows the signal to noise improves eight-fold in the latter case.

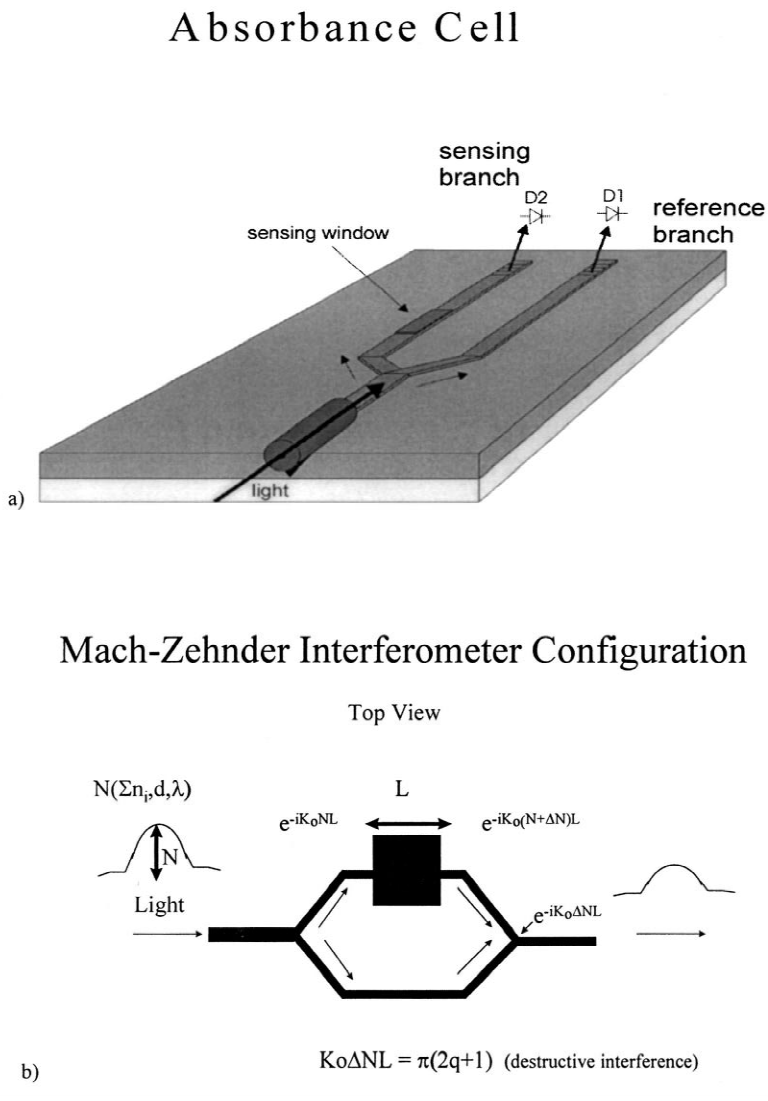

Fig. 10. Schematic illustration of planar waveguide structures for measurement of absorption (a) and refractive index (b).

5.2. Optical waveguide detectors

Integrated optical detectors for chemical sensing have interesting properties such as high sensitivity, small size, absence of electromagnetic interference, and, last but not least, ease of integration. The latter is a result of the fact that planar waveguides are usually made using thin films of oxynitride (SiON), layers that have an easily adjustable refractive index and that are readily deposited on silicon substrates. An additional advantage of planar waveguide detectors is that, since the optical energy extends only a small distance (several μm) in the adjacent fluid channel, they allow for measurements in extremely small sample volumes. Several devices have been proposed such as Mach–Zehnder interferometers [36], and absorption sensors [37] (see Fig. 10). These devices have several drawbacks, such as need for on chip modulation [38], and limited sensitivity, respectively.

A new optical refractometer using a spiral-shaped waveguide has recently been proposed [39]. The operation principle is based upon the fact that the transmitted light stays within curved waveguide structures with a certain radius depending on the refractive index contrast between the waveguide and the adjacent medium. Thus, the position in the spiral at which the transmitted light escapes from the waveguide is a precise measure for the refractive index of the medium. Using this structure, variations in the refractive index of the contacting medium of $\Delta n = 8 \cdot 10^{-6}$ can be detected, making this detector interesting for on-line detection in e.g. polymer separations.

6. Conclusions

Microchip technology is well suited for accurate fabrication of complex structures. Beside the fabrication of glass micro channels, it is demonstrated that connecting a microchip injection device to a fused-silica capillary can be done. SEM photographs proved that the connection is excellent, with extremely low dead-volume. The reproducibility in peak height and peak area of the electrokinetic injection was very good, with R.S.D. values better than 1.1%. An improved reproducibility with the microchip injection device compared to conventional injections has been demonstrated.

By using the GPSIC method, channels were made that are suitable for electrophoretic pumping. The geometry of the channels, unlike those etched in glass, is completely up to the user. For example, high aspect ratio channels that may minimize band broadening can be fabricated using DRIE in silicon, then formed into closed glass channels using GPSIC. Porous silicon and silicon black structures have potential as monolithic high surface area substrates for CEC. Porous silicon filled channels have been achieved. However, the characterization of passivated structures for CZE remains to be done.

DEEMO can be applied to the construction of microchannels and vials in plastics. This is attractive as structures first characterized in silicon become of interest for mass production. Additionally, while structures can be made in much cheaper plastic, all the advantages of machining silicon are retained. A possible drawback is the inconvenience of integrating detectors in plastic at the moment. Finally, the interesting potential of silicon to realize integrated optical detectors is illustrated with a novel optical refractometer.

It is a worthwhile endeavor to consider the advantages of working in silicon. Glass, while convenient and widely used, suffers from the limitations of the micromachining techniques available. Plastics are much more convenient for use in a disposable system. However, plastics currently must be molded, not micromachined. The randomness of polymer organization makes it unsuitable for precise microfabrication using wet chemical or dry etch methods, although photolithography and laser ablation remain possibilities.

Silicon remains the material that is most precisely and proficiently micromachined. High surface areas in silicon are easily achieved. Due to technologies such as DEEMO, designs prototyped in silicon can be easily transferred to cheaper materials such as plastics. In silicon, the potential for added value, such as integrated detectors, is much easier to realize. Therefore, it is unlikely that silicon has outlived its usefulness to μTAS development.

Acknowledgements

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